REMARKS

Pending Claims:

In this application, claims 2-13 have been canceled. Claims 1 and 14 have been amended. Claims 15—22 have been added. Entry of these amendments is respectfully requested.

New Claims

The rejections of the previous claims based on §102(b) relied upon Rodiger et al. (U.S. Patent 4,991,084). Those based on §103 relied upon Rodiger in view of Cooke et al. (U.S. Pub. No. 2002/0073380). Our new claims include several structure and process claims supported by the specification, each incorporating aspects of the invention that distinguish it critically from Rodiger. (The Cooke reference is irrelevant to our new claims.)

The Rodiger scheme routes data from source ports ("FIFO buffers," which correspond to processors) to destination ports ("basic storage modules (BSM)") in discrete chunks: "The output from each of the processors ... includes a request code signal and associated data signals or data packet." (Col. 1 lines 65—67.) The request code specifies the destination port to the data packet is to be routed. (Col. 2 lines 3—24.) Routing requests are made and processed on a packet by packet basis. When more than one request is pending to route data to a particular destination, then an arbitrator causes a selector to send a packet at a time in synchronization with a clock cycle, alternating among sources requesting a given destination (Col. 2 lines 25—57.)

The approach of our invention does not re-arbitrate each path at the end of each data packet, making it fundamentally different from Rodiger and similar schemes in several respects. Rather, when the present invention opens a connection from a source port to a destination port, that connection remains open until it is sent an explicit request to close. This is specifically claimed in revised claims 1b and 14c, which is sufficient to distinguish these claims from the cited prior art. By leaving the connection open in this way, a single source can send a large block of data to a given destination without interruption caused by other sources claiming the destination, which may occur at each re-arbitration. There are no discretized packets, and no restrictions that tie the amount of data sent in a block to the maximum amount that can be sent within a

given clock cycle. Our invention can transmit substantially more total information within a given amount of time because we only check routing information once for a given transmission, while Rodiger must check routing information for each individual packet of data.

Because Rodiger contains routes and sequences information at a data packet level, the concept of a particular source being "connected" to a chosen destination does not have meaning in the context of their invention. With our dedicated connections, the source port can take advantage of the knowledge of whether it is currently connected or not. The source might, for example, choose to dynamically reroute itself to a new destination if it learns that it has been systematically failing to connect to the current one. To implement this feedback to the sources, each destination sends to each source a connection status (claims 17, 20d). In the principal embodiment described in the specification, these acknowledgements are combined with a logical OR; this information is adequate feedback because the source already knows which destination it has requested.

Devices downstream of a switch can get overloaded with information to process, or they can fail. The Rodiger scheme does not address this situation. In our invention, an open connection path can be sent an XOFF signal to temporarily suspend data flow, and an XON signal to allow data flow to resume (claims 16, 21i, and 21j). A destination having no open path can be similarly instructed to refuse or allow connections (claims 16, 21k, and 21l).

An open connection can be set to close after a predetermined amount of time or upon some programmatic condition. For example, a connection that has been suspended with an XOFF signal might eventually time out and close. Similarly, connections can be closed upon the occurrence of specified programmatic conditions (claims 18 and 22).

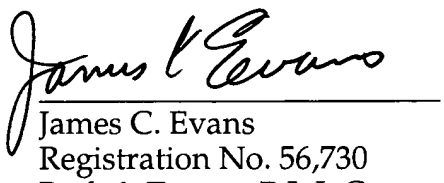
Finally, the Rodiger scheme is optimized for connecting computer processors to memory units (Col. 1 lines 53—58), giving rise to their need to arbitrate at the highly granular packet level. The demands on a switch controlling connections in a fibre optics communications system are different, and include the need to maintain open connections; to monitor whether a connection is open or not and modify system behavior in response; and to suspend and restore access to resources. Claim 19, which includes a Fibre Channel switch, makes this distinction explicit.

CONCLUSION

All of the claims remaining in this application should now be seen to be in condition for allowance. The prompt issuance of a notice to that effect is solicited.

Respectfully submitted,
COMPUTER NETWORK
TECHNOLOGY CORPORATION
By its attorneys:

Date: _____



James C. Evans
Registration No. 56,730
Beck & Tysver, P.L.L.C.
2900 Thomas Ave., #100
Minneapolis, MN 55416
Telephone: (612) 915-7006
Fax: (612) 915-9637